CLAIMS

WHAT IS CLAIMED IS:

1. A semiconductor memory comprising:

a plurality of memory cells having transfer transistors and driver transistors, respectively;

a plurality of word lines connected to gates of said transfer transistors, respectively;

a first driver circuit having a plurality of first buffers for generating voltages to be supplied to said word lines, respectively;

a plurality of first substrate lines connected to substrates of said transfer transistors and of said driver transistors, respectively; and

a second driver circuit having a plurality of second buffers for operating in synchronization with said first buffers to generate voltages to be supplied to said first substrate lines, respectively.

2. The semiconductor memory according to claim 1, wherein:

each of said second buffers supplies a voltage for lowering threshold values of said transfer and driver transistors to its corresponding first substrate line of said first substrate lines when a voltage for turning on said transfer transistors is supplied to one of said word lines;

each of said second buffers supplies a voltage for raising the threshold values of said transfer and driver transistors to said corresponding first substrate line when a voltage for turning off said transfer transistors is supplied to said one of said word lines.

3. The semiconductor memory according to claim 2, wherein

each of said second buffers supplies a power supply voltage to said corresponding first substrate line when the voltage for turning on said transfer transistors is supplied to said one of said word lines.

4. The semiconductor memory according to claim 2, wherein

each of said second buffers supplies a first voltage to said corresponding first substrate line when the voltage for turning on said transfer transistors is supplied to said one of said word lines, said first voltage being lower than a forward bias of respective pn junctions between a substrate, and sources and drains of said transfer transistors, and between a substrate, and sources and drains of said driver transistors.

5. The semiconductor memory according to claim 4, wherein

said first voltage is lower than a power supply voltage.

6. The semiconductor memory according to claim 4, wherein

said first voltage is higher than a power supply voltage.

7. The semiconductor memory according to claim 2, wherein

each of said second buffers supplies a ground voltage to said corresponding first substrate line when the voltage for turning off said transfer transistors is supplied to said one of said word lines.

8. The semiconductor memory according to claim 2, further comprising

a negative voltage generator for generating a negative voltage, wherein

each of said second buffers supplies said negative voltage to said corresponding first substrate line when the voltage for turning off said transfer transistors is supplied to said one of said word lines.

9. The semiconductor memory according to claim 8, wherein

each of said second buffers supplies a ground voltage to said corresponding first substrate line when the voltage for turning on said transfer transistors is supplied to said one of said word lines.

10. The semiconductor memory according to claim 1, comprising

a memory cell array composed of said memory cells, wherein

said first and second driver circuits are arranged on one side of said memory cell array.

11. The semiconductor memory according to claim 10, wherein

each of said second buffers of said second driver circuit is arranged between two first buffers of said first driver circuit.

12. The semiconductor memory according to claim 1, comprising

a memory cell array composed of said memory cells, wherein

said first driver circuit is disposed on one side of said memory cell array and said second driver circuit is disposed on the other side of said memory cell array.

13. The semiconductor memory according to claim 1, wherein:

said first substrate lines are connected to first substrate areas, respectively, each of said first substrate areas being formed in common for two adjoining memory cells of said memory cells; and

said second buffers are formed correspondingly to said first substrate areas, respectively.

14. A semiconductor memory comprising:

a plurality of memory cells having transfer transistors and load transistors, respectively;

a plurality of word lines connected to gates of said transfer transistors, respectively;

a first driver circuit having a plurality of first buffers for generating voltages to be supplied to said word lines, respectively;

a plurality of second substrate lines connected to substrates of said load transistors, respectively; and

a third driver circuit having a plurality of third buffers for operating in synchronization with said first buffers to generate voltages to be supplied to said second

substrate lines, respectively.

15. The semiconductor memory according to claim 14, wherein:

each of said third buffers supplies a voltage for lowering threshold values of said load transistors to its corresponding second substrate line of said second substrate lines when a voltage for turning on said transfer transistors is supplied to one of said word lines; and

each of said third buffers supplies a voltage for raising the threshold values of said load transistors to said corresponding second substrate line when a voltage for turning off said transfer transistors is supplied to said one of said word lines.

16. The semiconductor memory according to claim 15, further comprising

a booster for generating a boost voltage higher than a power supply voltage, wherein

each of said third buffers supplies said power supply voltage to said corresponding second substrate line when the voltage for turning on said transfer transistors is supplied to said one of said word lines; and

each of said third buffers supplies said boost voltage to said corresponding second substrate line when the voltage for turning off said transfer transistors is supplied to said one of said word lines.

17. The semiconductor memory according to claim 14, further comprising

a memory cell array composed of said memory cells, wherein

said first and third driver circuits are arranged on one side of said memory cell array.

18. The semiconductor memory according to claim 14, wherein

each of said third buffers of said third driver circuit are arranged between two first buffers of said first driver circuit.

19. The semiconductor memory according to claim 14, comprising

a memory cell array composed of said memory cells, wherein

said first driver circuit is disposed on one side of said memory cell array and said third driver circuit is disposed on the other side of said memory cell array.

20. The semiconductor memory according to claim 14, wherein:

said second substrate lines are connected to second substrate areas, respectively, each of said second substrate areas being formed in common for two adjoining memory cells of said memory cells; and

said third buffers are formed correspondingly to said second substrate areas, respectively.